Hardware Implementation and Phase Noise Analysis of Phase Locked Loop Frequency Synthesizer

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Abstract—*Phase Locked Loop is widely used in microprocessors and digital systems for generation of clock and synthesis frequency for communication system. Phase Locked Loop based frequency synthesizer composed of a phase frequency detector, a loop filter, a voltage controlled oscillator and a frequency divider. In this paper we will present the design, fabrication and phase noise analysis of a phase locked loop based frequency synthesizer. The system is implemented by using discrete surface mount devices. The synthesizer used in the system is ADF4002 from Analog Devices having a low noise digital phase frequency detector, a precision charge pump, a programmable reference divider (R divider) and a programmable feedback frequency divider (N divider). The charge pump, R divider and N divider are programmed externally through a serial peripheral interface (SPI) by writing date to the control of the device. The testing of the output of the system is tested by using Agilent Spectrum Analyzer, Tektronix 100 MHz arbitrary function generator and 500 MHz Digital Phosphor Oscilloscope (DPO). This paper will give a brief outline of the hardware design, fabrication, testing and study of phase noise of the system.*

1. INTRODUCTION

The phase locked loop (PLL) is a negative feedback control system. It uses a feedback loop for synchronization of phase and frequency of output with the input reference signal. The phase frequency detector (PFD) detects the difference between the phases of input reference with the voltage controlled oscillator (VCO) output frequency. The output of the PFD is proportional to the difference of the two input frequencies [1]. In ideal steady state condition, the difference between the phase and frequency of the controlled oscillator and reference frequency becomes zero [2]. The PFD output is applied to loop filter (LF) and produces a signal to control the VCO that generates the output frequency according to the variation of the control voltage. In the locked condition, the output of the PLL frequency is in phase and frequency of the input signal. The frequency of the PLL can be synthesized by using a frequency divider (FD) network in the feedback loop.

The major problems in designing such a system are frequency accuracy, frequency step, tuning range and phase noise (PN) and spur [3]. In the process of frequency synthesis, PN is generated in the system and hence predicting the PN in the system and accurate modeling of such system in component level is essential [4]. Any jitter or PN in the output of a PLL degrades the performance of the system [5]. The ultimate goal of PLL frequency synthesizers is to generate precise and stable output frequencies with fast switching and minimal spurious and PN [6 – 7]. By properly designing the LF, a desired balance can be achieved between PLL spurious noise levels.

2. SYSTEM DESIGN AND FABRICATION

The block diagram of the system is shown in Fig. 1. It consists of a frequency synthesizer (ADF4002), a passive LF, a VCO (MC100EL1648) and a reference frequency generator. The synthesizer consists of low noise PFD, a programmable R divider, a feedback frequency N divider and a precision CP [8]. The R divider divide the input reference frequency to produce the reference clock for the PFD. It has the division ratio from 1 to 16383. The N divider is a 13-bit counter and has a division ratio from 1 to 8191. The PFD compares the phase and frequency of the signal from R and N divider and produces an output control signal proportional to the phase and frequency difference between them. The registers of the synthesizer chip can be programmed externally by using serial peripheral interface (SPI) through writing to CLK, DATA and latch enable (LE) control of the device. The maximum allowable clock frequency is 20MHz. The system is interfaced to personal computer through microprocessor 8085 via RS232 interface. The synthesizer has an inbuilt 24-bit shift register where the data is clocked down on each rising edge of the clock signal. Initially, the data is clocked with most significant bit and transferred from the shift register to one of the four latches available in the device on the rising edge of LE. The destination latch of the synthesizer is determined by the state of the two least significant bits in the shift register. An 8085 microprocessor is used to transfer the programmed data to the synthesizer. An external parallel tank circuit consisting of an inductor and a capacitor is used with the VCO to adjust the frequency. The varactor diode (MMBV609) with a parallel

inductor is connected into the tank circuit to provide a voltage variable capacitance for the input of the VCO. A low power VCO with a supply voltage 5V is used in the system. The gain of the VCO is 30 MHz/V and the tuning range is 128 – 256 MHz.

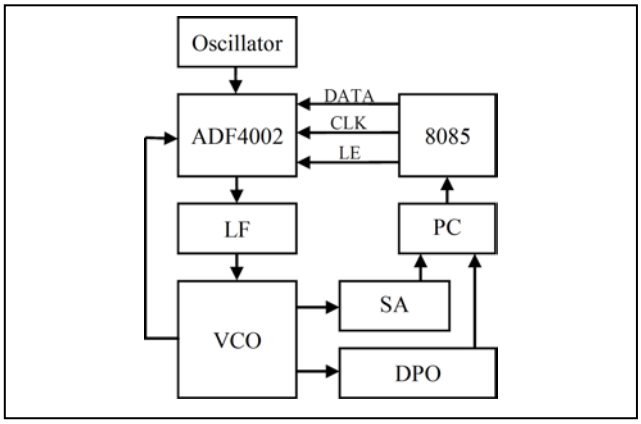

Fig. 1: The block diagram of the PLL frequency synthesizer

3. HARDWARE DESIGN AND FABRICATION

The hardware of the system is designed using SMD technology. A double sided glass epoxy printed circuit board (PCB) is used to populate the SMD components using hot air soldering technology. The schematic and layout of the PCB is designed in Novarm Dip Trace PCB design software. The layout of the PCB is transferred to one side of the PCB using tonner transfer method. The PCB is then etched by using $FeCl_3$ solution at room temperature. The other side of the PCB is grounded to minimize noise effect of the system. A power supply unit is also designed and fabricated for the system. The fabricated PLL synthesizer board is shown in Fig. 2.

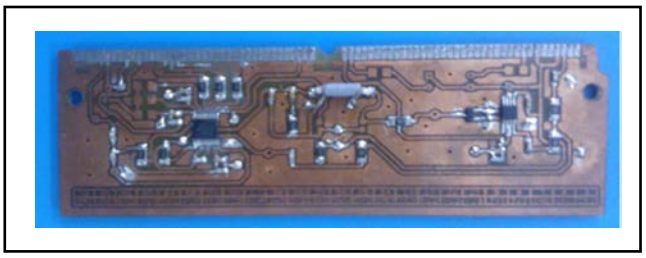

Fig. 2: Fabricated PLL synthesizer board

4. THE SOFTWARE

The software required for configuration of the system is developed on OshonSoft 8085 microprocessor simulator integrated development environment. The developed programme is transferred to microprocessor from the PC through RS232 serial port and finally the data was transferred to the registers of the synthesizer through the parallel port of the system. The device is configured using initialization latch method. The timing signal generated by microprocessor for clock, data and LE to configure and test the system and recorded by DSO is shown in Fig. 3.

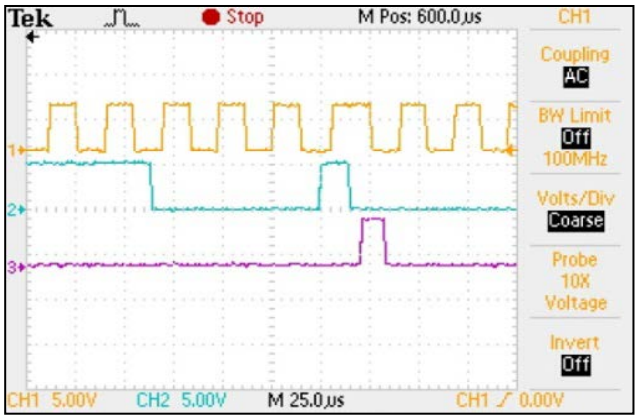

Fig. 3: Timing signal generated by microprocessor

5. RESULT AND DISCUSSION

The testing of the system has been carried out by using Agilent Spectrum Analyzer (Model: N9320B, Frequency range 9 KHz – 3 GHz), Tektronix 100 MHz arbitrary function generator (Model: AFG 3012, 1 GS/s), Tektronix Digital Phosphor Oscilloscope (Model: TDS 3052, 500 MHz, 2.5 GS/s). The output spectrum of the system (Fig. 4) shows that the output power is -9.21 dBm when the system is locked 226.3 MHz. The recorded PN is -63.0 dBc/Hz and -114.4 dBc/Hz at 1 Khz and 1 MHz respectively from the carrier for the same locked state. Fig. 5 amd Fig. 6 shows the PN spectra of the system.

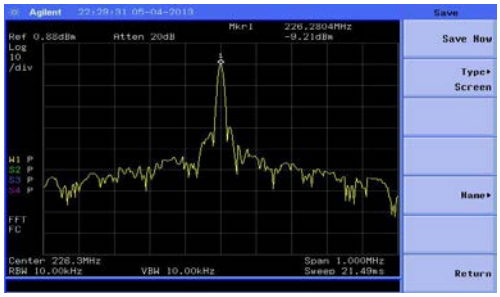

Fig. 4: Output spectrum of frequency synthesizer at 226.3 MHz

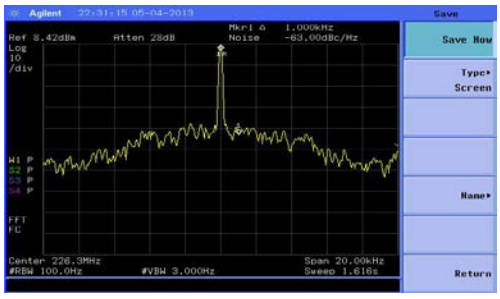

Fig. 5: Phase Noise at 1 KHz offset from the carrier when the system is locked at 226.3 MHz

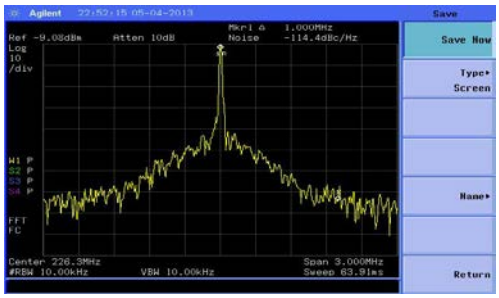

Fig. 6: Phase Noise at 1 MHz offset from the carrier when the system is locked at 226.3 MHz

Again the measured output power is –8.20dBm (Fig. 7) and PN is -63.43dBc/Hz and –107.5dBc/Hz respectively at 1 KHz and 1 MHz offset from the carrier when the system is locked at output frequency 240.4 MHz (Fig 8 & 9).

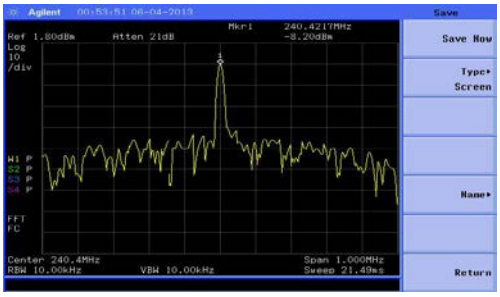

Fig. 7: Output spectrum of frequency synthesizer at 240.4 MHz

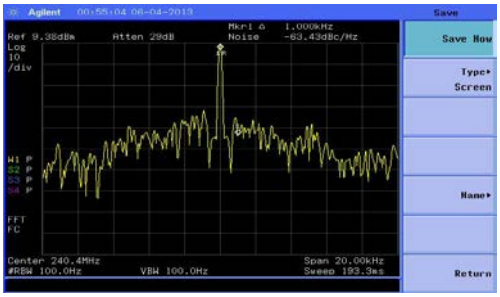

Fig. 8: Phase Noise at 1 KHz offset from the carrier when the system is locked at 240.4 MHz

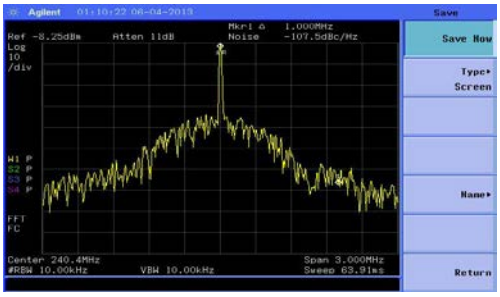

Fig. 9: Phase Noise at 1 MHz offset from the carrier when the system is locked at 240.4 MHz

6. CONCLUSION

Design and analysis of PLL frequency synthesizer is very challenging because several parameters have to be taken into consideration simultaneously. Extreme care should be taken during the design and it requires fine tuning to improve the noise parameter. The synthesizer can be tuned to produce frequencies upto 1.1 GHz with minimum noise and hence can be used in FM, line of sight ground to aircraft communication, Mobile communication systems.

7. ACKNOWLEDGEMENTS

Author is thankful to the University Grants Commission, Government of India for partial support towards the work. He is also grateful to the Head of the Department of Electronics and Communication Technology, Gauhati University, Guwahati for providing infrastructural support for implementation of the present work. He is also thankful to Analog Devices, USA for supplying few SMD components free of cost and time to time technical support towards implementation of the work.

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